My current research focus includes high performance computer/computing (HPC) systems, machine learning (ML), HPC and ML in healthcare technology, and performance and power evaluation. I have been conducting innovative research to develop power-aware HPC systems since I was a PhD student at Florida Atlantic University (FAU). As a principle investigator (PI) at Wichita State University (WSU), I have received several research grants from the WSU internal sources. I have published more than 30 refereed journal articles, book chapters, more than 20 peer-reviewed conference papers, and more than ten technical articles out of my research work. I have been serving the research communities as a panel reviewer, panel presenter, invited speaker, journal reviewer, technical/international program committee member, and numerous volunteer activities in my university.

At the Computer Architecture and Parallel Programming Laboratory (CAPPLab) at WSU, I have been working on important research projects. In the project funded by ANL (08/2022-08/2023), we are optimizing applications on Exascale machines using the Portable, Extensible Toolkit for Scientific Computation (PETSc) and the Data Management Network (DMNetwork) libraries that are of interest to the DOE. We generate realistic traffic data in Hierarchical Data Format 5 (HDF5) for selected cities using SUMO netconvert (a network simulator) and develop/update PETSc subroutines for parallel HDF5 data processing. The resulting code development is included into the PETSc library, benefiting the scientific community in large. In the project funded by DOE Visiting Faculty at Lawrence Berkeley National Laboratory (LBNL) (06/2020-08/2021), we automate code generation through a reliable methodology for generating graphic design system (GDS) code files of matrix-matrix multiplication (MMM). We synthesize the Pythonic code in large.

During my undergraduate study at Bangladesh University of Engineering and Technology, an ABET accredited institution. I developed a hardware description language to facilitate "Computer Aided Design of Circuits for Counting of Current Distributions". This undergraduate research work was submitted in partial fulfillment of the requirements for the degree inspired by my undergraduate research work that I pursued my graduate in Computer Engineering at FAU.

Modern multiprocessors use cache-coherent multiprocessor systems with a cluster-based architecture which is a variation of cache-only memory architecture (COMA). In this architecture, snoopy protocol (when the number of processors per cluster is small). Clusters are